AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application.

Listing of Claims:

Claim 1. (currently amended) A method, comprising:

transferring a data block between a flash memory and a memory controller;

computing an ECC for said data block while transferring the data block; and

selectively storing the ECC in a plurality of registers using a switching mechanism, the storing of the ECC occurring concurrently with ~~while~~ transferring the data block.

Claim 2. (Original) The method of claim 1, wherein transferring the data block comprises transferring the data block between a NAND Flash memory and the memory controller.

Claim 3. (Previously Presented) The method of claim 1, wherein selectively storing the ECC further comprises

storing a first portion of the ECC in a first register; and

storing a second portion of the ECC in a second register if the first register is full.

Claim 4. (Previously Presented) The method of claim 3, wherein storing in a second register comprises selecting the second register using the switching mechanism.

Claim 5. (Original) The method of claim 1, wherein computing the ECC comprises performing the exclusive-or function.

Claim 6. (currently amended) A system, comprising:

a flash memory;

a controller coupled to the flash memory;

a switch coupled to the controller; and

said controller is configured to shift a data block between the flash memory and the controller and compute an ECC for said data block, said controller computing said ECC for said data block concurrently with shifting said data block between the flash memory and the controller ~~while computing an ECC for said data block~~; and

said system is configured to selectively store the ECC in a plurality of registers using the switch, while the controller shifts the data block.

Claim 7. (Original) The system of claim 6, wherein the flash memory is a NAND Flash memory.

Claim 8. (Previously Presented) The system of claim 6, wherein the system is configured to

store a first portion of the ECC in a first register; and

store a second portion of the ECC in an alternate register if the first register is full.

Claim 9. (Previously Presented) The system of claim 8, wherein the controller is configured to transfer contents of all registers to memory if all registers are full.

Claim 10. (Previously Presented) The system of claim 8, wherein the switch configured to select the alternate register.

Claim 11. (Previously Presented) The system of claim 6, wherein the controller is configured to compute the ECC while performing the exclusive-or function.

Claim 12. (Previously Presented) A system comprising:

a means for storing a data block;

a means for controlling the data block;

a means for computing an ECC of the data block;

a means for shifting the data block between the means for storing and the means for controlling while computing an ECC for said data block; and

a means for selectively storing the ECC in a plurality of registers while shifting the data block.

Claim 13. (Original) The system of claim 12, wherein the means for storing is a NAND Flash memory.

Claim 14. (Previously Presented) The system of claim 12, wherein the means for selectively storing the ECC is configured to

store the ECC in a first register; and

store the ECC in an alternate register if the first register is full.

Claim 15. (Previously Presented) The system of claim 12, wherein the system is configured to transfer contents of at least one register to memory if all registers are full.

Claim 16. (Previously Presented) The system of claim 14, wherein the means for selectively storing the ECC is a switch configured to select the alternate register.

Claim 17. (Previously Presented) The system of claim 12, wherein the system is configured to compute the ECC while performing the exclusive-or function.

Claim 18. (Previously Presented) A memory controller configured to couple to a memory, comprising:

a memory interface;

an ECC engine configured to compute an ECC while transferring a data block between the ECC engine and memory; and

a switching mechanism coupled to the ECC engine, the ECC engine configured to selectively store the ECC in a plurality of registers using the switching mechanism, while transferring the data block.

Claim 19. (Previously Presented) The memory controller of claim 18, further comprising:

a register bank coupled to the switching mechanism, comprising at least one register;

wherein the ECC engine configured to store the ECC in a register selected by the switching mechanism, the register having space available for ECC storage.

Claim 20. (Previously Presented) The memory controller of claim 18, wherein the controller is configured to transfer a data block while transferring the data block between the ECC engine and a flash memory.

Claim 21. (Previously Presented) The memory controller of claim 18, wherein the controller is configured to transfer a data block while transferring the data block between the ECC engine and a NAND Flash memory.

Claim 22. (Previously Presented) The memory controller of claim 18, wherein the ECC engine is configured to transfer a data block by reading the data block from memory.

Claim 23. (Previously Presented) The memory controller of claim 18, wherein the ECC engine is configured to transfer a data block by writing the data block to memory.

Claim 24. (Previously Presented) The system of claim 8, wherein the first register is in the controller.

Claim 25. (Previously Presented) The system of claim 8, wherein the alternate register is in the controller.

Claim 26. (Previously Presented) The system of claim 10, wherein the switch is in the controller.